Swiss Nanoscience Institute
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Strained Germanium Quantum-Well Transistors for Integrated Cryogenic Spin Qubit Readout

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Building a quantum computer that can solve real-world problems will require the integration of many highly coherent qubits. Hole-spin qubits in planar germanium quantum wells are among the most promising candidates for this goal, combining fast electrical control, compact device geometry, and excellent performance in a semiconductor platform. As this technology advances, one of the main remaining challenges is readout: the quantum state of each qubit must be converted into a small electrical signal and detected quickly and reliably. At present, this still depends strongly on external wiring and amplification hardware, which becomes increasingly difficult to scale as the number of qubits grows.

This PhD project aims to explore strained Ge/SiGe quantum-well transistors as integrated cryogenic readout devices for hole-spin qubits. By operating amplification and signal routing closer to the quantum device, the project seeks to enable more compact and scalable readout architectures at very low temperatures. By combining advanced material growth, nanoscale fabrication, and cryogenic device physics within a single material platform, the work aims to develop new concepts for scalable quantum hardware. More broadly, it will strengthen planar germanium as a platform for integrated quantum nanoelectronics and help open a path towards large-scale semiconductor quantum processors.

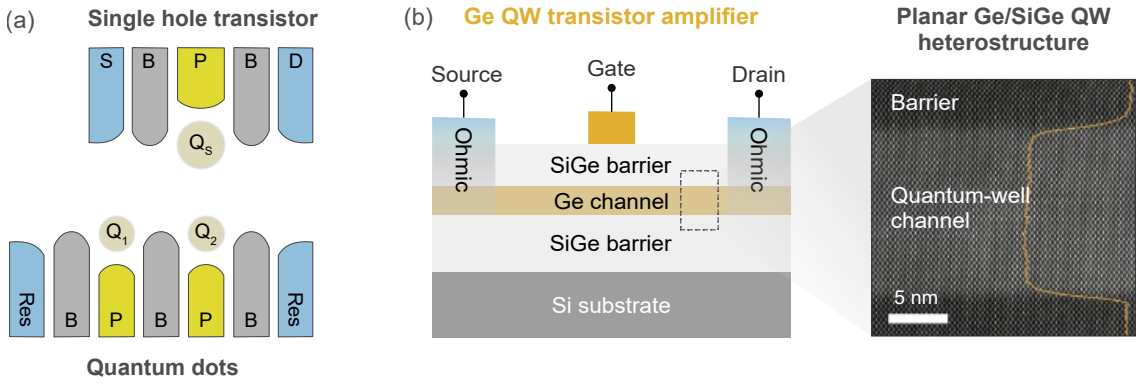

Figure 1: *(a) Schematic of a double quantum dot with single hole transistor readout. (b) A Ge quantum-well transistor architecture for integrated spin qubit readout and the corresponding heterostructure.*

Requisites: The candidate must have Master studies in nanoscience, physics or any related engineering. Previous experience in fabrication or transport measurements is desired but not compulsory.