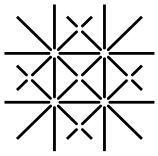

Universität Basel

Master's Thesis

Quantum Transport in Templated Indium Arsenide Nanowires

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April 2020

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Abstract

A possible way to build a fault tolerant quantum computer is by using topological qubits. 1D indium arsenide (InAs) nanowires (NW) are a promising medium to host topological qubits. With the vision of building a fault tolerant quantum computer, it is interesting to gain a deeper understanding of one dimensional InAs NW. In this thesis, templated InAs NW grown by molecular beam epitaxy are characterized using a field effect transistor configuration. To isolate the gates from the NW a dielectric material is required. The quality of the dielectric is very important, because trapped charges in the oxide will affect the stability of the device. Therefore, in this thesis it was investigated whether to use HfO_2 or Al_2O_3 as a dielectric. Similar mobilities were found, but the smaller hysteresis and the more reliable fabrication of the devices suggested using HfO_2 for further device fabrications. The system has been developed further in order to increase the potential to see ballistic transport. By measuring the device at 4.2 K, signs of ballistic transport were measured. For another device, the process of fabricating five gates of width 30 nm and a separation of 40 nm was created, in order to further investigate the InAs NW.

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QUANTUM TRANSPORT IN TEMPLATED INDIUM ARSENIDE NANOWIRES

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April 2018

Contents

1 Motivation

Generally, there are two sources which are limiting the ability of computers to solve large problems: time and space. [1] Quantum physics gives the potential to build a computer which can perform a large number of computing operations in parallel. Therefore, it can execute certain computational tasks faster than a classical computer and can solve problems in a matter of days, which would take billions of years with today's supercomputers. [2, 3] The basis of classical computers are bits, which have two states 0 and 1. For quantum computers the basis are quantum bits (qubits), which can exist in any arbitrary superposition of $|1\rangle$ and $|0\rangle$. [4] The main barriers of quantum computing are noise and decoherence. The imperfections which occur in the execution of operations on the qubit is associated with noise. When the qubit becomes entangled with the environment decoherence arises because the environment is a bigger, uncontrolled system. To overcome these obstacles, there are two approaches suggested. [5] One is to isolate the quantum computing completely from the environment and minimize noise by using protocols for quantum error correction (QEC). In practice, it is not possible to fully decouple any quantum system from the environment, in order to reduce decoherence. The interaction between the coherent qubit and the environment leads to a suppression of the stable quantum state, on which a quantum computer relies on. For short calculations, this is less of a problem. But if the coherence time of the qubit is smaller than the calculation time, the likelihood of an error strongly increases. When scaling up to larger numbers of qubits, this problem also scales up and the probability of having a decohere qubit becomes almost 1. To reduce the errors, QEC is used. It is predicted that QEC will require the major resources of quantum computers. [6] The second approach is to use topological quantum computation. It uses non-abelian quantum states of matter to store and manipulate quantum information in a nonlocal manner, which protects the information from noise and decoherence. [5, 6] This has resulted in a large interest in Majorana fermions (MFs), which are a possible way to store topological quantum computation information in multiple non local Majorana zero modes (MZM). [5]

With the vision of building a fault tolerant quantum computer, it is interesting to gain a deeper understanding of the material used in Kitaev's theoretical work [7]. We therefore focused on the characterization of indium arsenide (InAs) nanowires (NW). In addition, our NW are grown by selective area growth (SAG), which is a scalable process and therefore an advantage in order to build a quantum computer. For the characterization, different samples were fabricated, where the material of the dielectric layer was varied between hafnium(IV) oxide (HfO_2) and aluminium oxide (AL_2O_3). Different gates were fabricated and also the

dielectric layer thickness was varied. All of this was done to study the electrical transport in selective area grown InAs NW at 4 K. The master thesis was done in combination with a Projektarbeit. The Projektarbeit focus lies on the fabrication techniques used.

2 Introduction

In the following section, numbers about the current competing quantum computer architectures are given, to summarize the achieved results in the different architectures. Due to the topic of this thesis, it will be focused on topologically protected states. The potential of such states for quantum computing is quantitatively described. Electrical transport is also important to understand the measurements and results of this work. Therefore, the used concepts are described.

2.1 Today's Qubits

Today, research is done in many competing qubit architectures. A short overview is presented in Table 1.

Qubit	Coherence Time	#Qubits	Gate Operation Time	Gate Fidelity
SC	100 μm [8]	53 [2]	10-100 ns [9]	$> 99\%$ [8, 9, 10]
QD	20 μm [11]	4 [12]	100 ns [11]	$> 99\%$ [11, 13, 14]
Ion	> 10 min [15, 16]	7 [17]	1.6 μs [18]	$> 99\%$ [15, 19, 20, 21]
Topol.	est. 200 ns-7 min [22]	0	est. 1 μs [23]	est. $> 99\%$ [23]

Table 1: An overview of important numbers for different qubit architectures, such as superconducting (SC), quantum dot (QD), ion and topological qubits. The values for topological qubits are estimated values, because there has been no topologically protected qubit realized, so far. Table taken and updated form [24].

In general, two approaches for a practical quantum computer are pursued. One is to use easier-to-build qubits with a relatively short life time but in a large quantity and dealing with errors by using QEC. The other is to use topological qubits, which theoretically have a lower error rate and a much longer coherence time. This approach would need less QEC, and therefore also fewer physical qubits to build a quantum computer as powerful as with the first approach. The big disadvantage of using topological qubits is that no working topological qubit has been realized so far. In comparison, superconducting (SC) qubits already have been realized and extensively studied (Table 1). Nevertheless, if a topological qubit can be built, it could hold many advantages. [4, 25, 26]

2.2 Topologically Protected States

To create a topological qubit several kinds of quasi-particles and systems have been proposed, where Majorana fermions seem to be experimentally the most promising approach. [27] The idea of encoding quantum information in topological properties of matter and having quantum gates depending on the topology of the evolution, was first introduced by Kitaev. [7] The realization of a system described by Kitaev would inherently protect the quantum computation from local perturbation if the topological phase remains intact, and would not require QEC. For a system with topological phase, the ground states are degenerate and depend on the topology. Kitaev noticed that one can look at QEC-surface codes as spin lattice models, which have elementary excitations in exotic quasiparticles, called anyons. Anyons generalize the statistics of fermions and bosons. [7] To create a topological qubit, one uses anyons and manipulates the elementary excitations and therefore encodes the quantum states in the global properties of the system. To implement quantum gates, one can move the anyons along non-contractable paths. The gates are the same as long as the paths are topologically equivalent. [27] The idea of using anyons seems to be promising, but where should we look for such quasi particles?

If two identical particles are exchanged, the local physics remains unchanged. In 3D this means that only bosons and fermions can exist as a point like particle. In terms of wavefunctions the exchange is described by a phase of 0 or π. When the dimensionality is reduced to 2D, the topology of space-time evolution is changed. [27] This can be illustrated by considering two exchange processes with different paths (λ_1 and λ_2), a schematic can be seen in Figure 1.

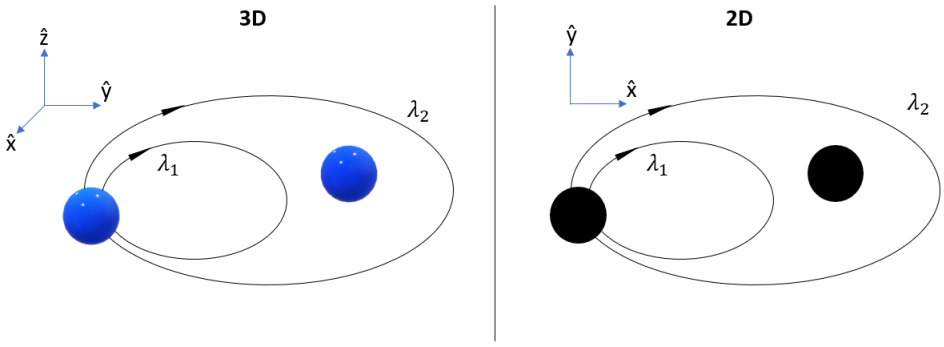


Figure 1: An illustration of the exchange process of particles in two and three dimension. The black arrows indicate the particle exchange. In 3D (left), λ_2 is contractible to λ_1, and λ_1 can be contracted to a point. This means that both paths have the equivalent topology. Whereas in 2D (right) this is no longer possible for the path λ_2. This means that the two paths are topologically inequivalent. Figure taken from [27].

In 3D both paths are contractable to a point, which leads to the following condition for the wavefunction: $\psi_{3D}(\lambda_1) = \psi_{3D}(\lambda_2) = \psi_{3D}(0)$. When one particle encircles the other twice one represents the evolution of the system as $\psi_{\lambda_2} = R^2\psi(0)$, with R being the exchange operator. Due to the contractibility of the loop $R^2 = 1$, which leads to $R = \pm 1$, which are either bosons or fermions. In 2D the path $\psi(\lambda_2)$ is no longer contractable to a point and therefore the wavefunction must fulfil: $\psi_{2D}(\lambda_2) \neq \psi_{2D}(\lambda_1) = \psi(0)$. In addition, R can now be represented by a unitary matrix or a complex phase. So, the exchange of non-abelian particles in 2D gives rise to a bigger range of statistical behavior and the exchange operator is no longer generally commutes. This has the consequence, that the orientation of the exchange matters. The only conditions R needs to satisfy are the one of the mathematical braid group. The braid group describes all the topologically distinct evolutions of point like particles in 2D. Due to the description of the 2D statistics in terms of the braid group, the existence of anyons is allowed. These anyons are called non-abelian anyons. This claims, that it needs to be looked at lower dimensional systems in order to build a topological qubit. [27]

Topological states of matter can be divided into two groups. One consists of states which are topologically protected by symmetry. These are called symmetry-protected topological (SPT) states. The second group are states with intrinsic topological order. In this thesis we focus on the SPT states, which include topological insulators, superconductors and integer quantum Hall states. They are classified as SPT states because of symmetries of time-reversal, symmetries of charge conjugation, and symmetry from the crystal lattices, which are systems of non-interacting fermions. SPT states do not support anyons as intrinsic quasiparticle excitation, except if the system has defects like lattice dislocations, vortices in SC, or domain walls in states of matter. All these defects give rise to the potential to bind localized zero energy modes, which are described in SC by Majorana fermions. Majorana zero modes behave like non-abelian anyons, but they are the most complex kind of anyons in SPT states of fermions. MZM are not universal for quantum computation, nevertheless they are probably the most experimentally achievable anyons. [27]

The first MF were proposed on non-abelian anyons in a 2D systems in 1997. [25] It was theoretically shown that in a two-dimensional p-wave superconductor, MF exist on vortices. The problem is, there are no suitable p-wave superconductors in nature. In 2000 Kitaev proposed a new way to realize MF by combining a 1D semiconductor system such as nanowires with a s-wave superconductor in proximity, where the MF would occur at the ends of the quantum wire. [7] Kitaev's idea has the advantage that nanowires and s-wave superconduc-

tors i.e. are widely available. [7] According to Kitaev there are two kinds of errors occurring on quantum states. One is a classical error, which flips the j^{th} qubit from $|0\rangle$ to $|1\rangle$ or vice versa. The other is a phase error which changes the sign of all the states with the j^{th} qubit equal to $|0\rangle$ relative to the states with the j^{th} qubit equal to $|1\rangle$. Imagine each qubit is a site which can be either occupied by an electron ($|1\rangle$) or empty ($|0\rangle$). Single classical errors are not allowed due to electric charge conservation. Only if two errors happen simultaneously, classical errors are still possible. This would implement that an electron needs to jump from one site to the other. This jump can be made less likely or even forbidden by separating the two sites far apart from each other, and the medium in between providing an energy gap. [22] This does not affect the phase errors. Phase errors are described by $a_j^\dagger a_j$. While having different electron configurations, one has different energies and therefore different phases over time, which results in decoherence. If we look at a nanowire, we can describe each fermionic site as a combination of creation and annihilation operator $a_j^\dagger$ and a_j. [7] Then Majorana operators are defined as:

$$c_{2j-1} = a_j + a_j^\dagger, \qquad (j = 1, ..., N) \tag{1}$$

$$c_{2j} = \frac{a_j + a_j^\dagger}{i} \tag{2}$$

If we have the operator c_{2j-1} for one site and c_{2j} for the other, then the phase error is equal to Equation 3, and unlikely to occur.

$$a_j a_j^\dagger = \frac{1}{2}(1 + i c_{2j-1} c_{2j}) \tag{3}$$

The two Majorana sites would have to interact with each other, which is possible to avoid. This leads to the statement that an isolated Majorana fermion is immune to classical errors and also to phase errors. [7]

2.2.1 Designing a System for Majorana Fermions

In this section, it will be described how to construct a system which should give rise to MF. Let's consider a 1D semiconductor quantum wire with strong Rashba spin-orbit coupling (α_R), a magnetic field (B) and a s-wave superconductor in proximity to the wire. A schematic can be seen in Figure 2 .

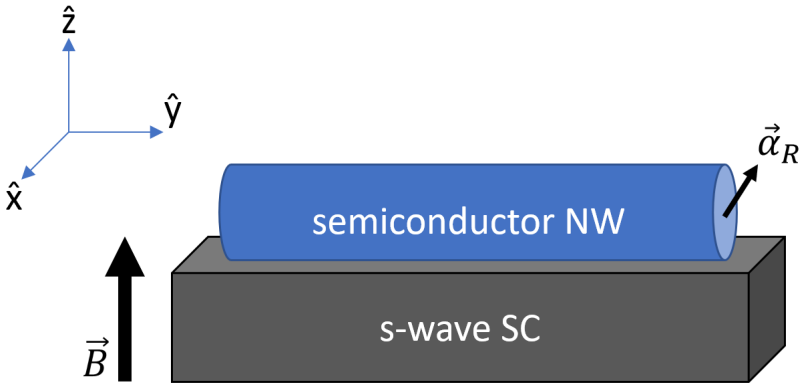


Figure 2: An illustration of a possible system, which in theory gives rise to unpaired MF. A semiconductor nanowire with strong Rashba spin-orbit coupling is placed in proximity to a s-wave superconducting material. Perpendicular to the resulting effective magnetic field B_{SO}, a magnetic field B is applied, here in the direction of z. Figure inspired by [28].

The Hamiltonian of the semiconductor nanowire (NW) in Figure 2 is given by:

$$H = H_{kin} + H_{SO} + H_Z + H_{SC}, \tag{4}$$

with H_{kin} the kinetic energy and chemical potential term, H_{SO} the spin orbital term, H_Z the Zeeman term arising from the applied magnetic field, and H_{SC} the superconducting term arising from the s-wave superconductor close to the nanowire. [28]

To understand Equation 4 better we will look into five different cases. First, when there is no magnetic field applied ($\Delta_Z = 0$) and no s-wave superconducting material ($\Delta_{SC} = 0$), the dispersion relation is split in momentum space due to the effective magnetic field from the Rashba spin-orbit coupling, which separates the opposite spins of the electrons, as seen in Figure 3a [29]. If the NW has no spin-orbit coupling ($\alpha_R = 0$) and $\Delta_{SC} = 0$ then the dispersion relation can be split in energy due to the Zeeman effect, illustrated in Figure 3b. When having spin-orbital coupling and a magnetic field applied ($\Delta_{SC} = 0, \Delta_Z \geqslant E_{SO} \neq 0$) the dispersion relation will be a mix of the two cases discussed before, so the bands will split in energy due to Zeeman effect and in momentum due to spin-orbit coupling. This can be seen in Figure 3c. For the case when there is also an s-wave superconductor in close proximity to the semiconductor NW ($\Delta_Z, \alpha_R, \Delta_{SC} \neq 0$), then the dispersion relation will look as in Figure 3d, where the Δ_{SC} opens up a superconducting gap. [28]

Depending on the relation between the Zeeman field (E_Z) and Δ_{SC} the gap evolves differently. If $\Delta_Z < \Delta_{SC}$ the dispersion relation looks like one of a trivial superconductor (Figure 3d), for $\Delta_Z = \Delta_{SC} = E_{SO}$ the gap is closed (Figure 3e), and for $E_z > \Delta$ the bands

are inverted because the gap opens up again. The last of these three scenarios is the goal in order to create MFs, because then one enters the topological regime, resulting in creation of a MF as zero energy bound states at both ends of the wire. [28]

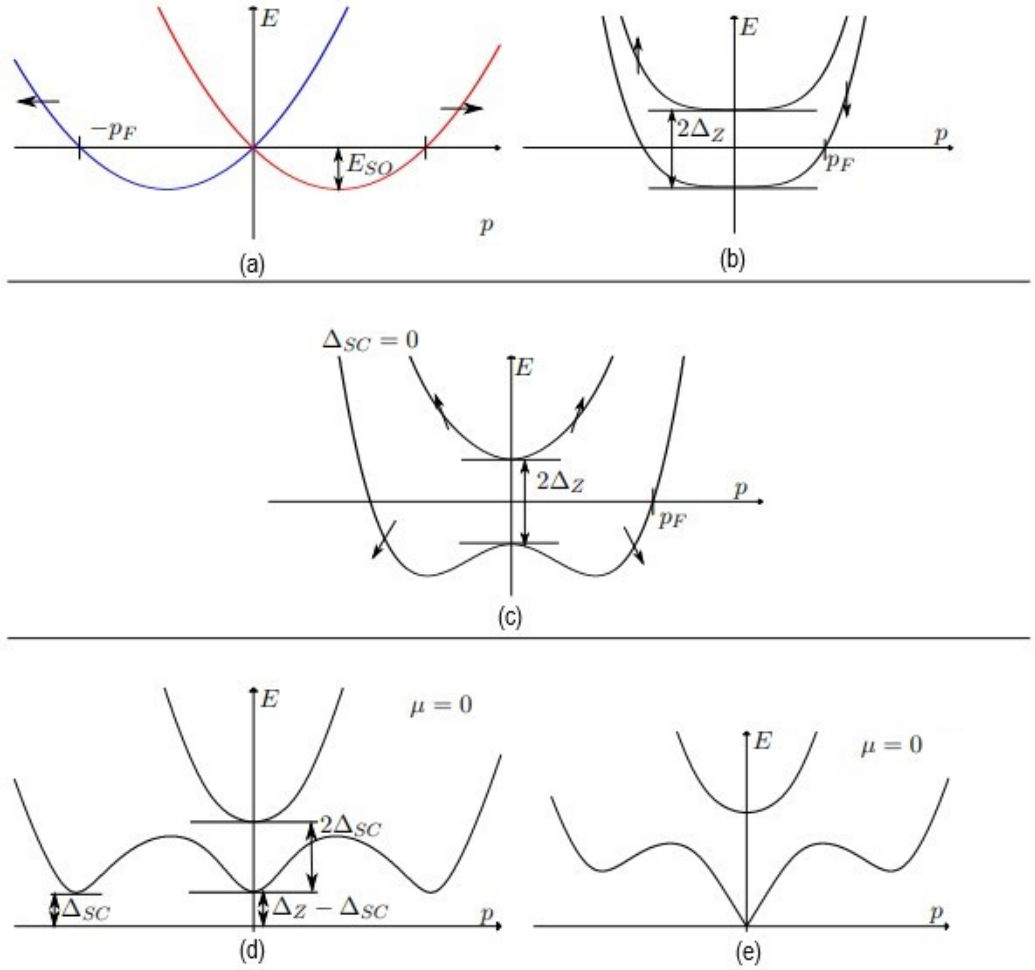


Figure 3: Dispersion relations for the five different cases, with the spin marked in a, b, and c. **(a)** The band splitting in momentum space due to E_{SO}, with $\Delta_Z = \Delta_{SC} = 0$. **(b)** Here, the bands are split in energy due to the magnetic field applied $\Delta_{SC} = \alpha_R = 0, \Delta_Z \neq 0$. **(c)** In case of strong Rashba spin-orbit interaction and a magnetic field applied the bands split in energy and momentum ($\Delta_{SC} = 0, \Delta_Z \geqslant E_{SO} \neq =$). **(d)** If $\Delta_Z, \alpha_R, \Delta_{SC} \neq 0$ and $\Delta_Z^2 \neq \Delta_{SC}^2 + \mu^2$, then the dispersion shows a gap in the energy spectrum. **(e)** In case of $\Delta_Z = E_{SO} = \Delta_{SC} \neq 0$ the dispersion no longer shows a gap. [28, 30]. Figure taken from [28] and modified.

In conclusion, the right combination of the ingredients is important to enter the topological phase. Another important part is the relation between the chemical potential and the Zeeman splitting. This is described by the following equation:

$$E_Z > \sqrt{\Delta^2 + \mu^2}, \tag{5}$$

with μ being the chemical potential in the wire, where $\mu = 0$ is set to be the lowest energy of a 1D subband at $B = 0$. [31] A visualization of Equation 5 is shown in Figure 4. One possible usage of materials would be InAs for the NW and aluminium as a superconducting material. [32]

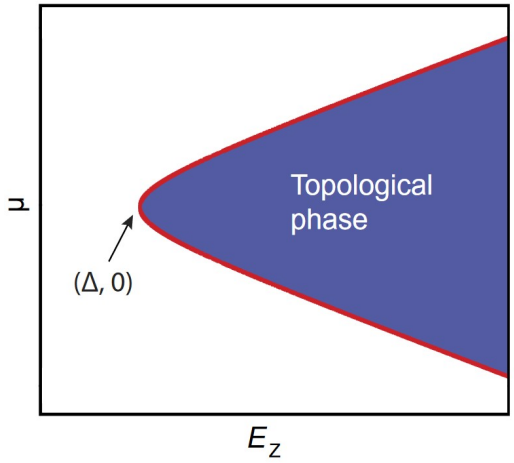


Figure 4: Visualization of Equation 5. Images taken from Chen et al. [31] and modified.

2.2.2 How to use Majorana Fermions for Quantum Computing

In case of a successful creation of MFs, the next step is to use those MFs for quantum computing. For one topological qubit one needs two pairs of MFs. Gate operations on the qubits can be performed in two ways, either by physically manipulating the MFs or by a measurement-based approach. For physical manipulation of the MFs one needs networks of T or Y shaped NW to perform braiding in order to implement gate operations. The measurement-based approach uses successive parity measurements on groups of MFs. This has the same effect as braiding, but without the need of T or Y shaped NW and physical movement of the MF. [33, 34] The fabrication of high-quality NW, which do not need to be T or Y shaped simplifies the fabrication process. From MFs one can build a Clifford gate. [35] The availability of only a Clifford gate does not make a universal quantum computer, which is a disadvantage of MFs. A solution for this is to combine it with a single non-Clifford gate which is not topologically protected, in order to have a universal quantum computer. [27] Going into more detail about how to use MFs for quantum computing is out of scope of this work. More details can be found in [23, 35, 36, 37].

2.3 Electrical Transport

In a metal (conductor), valence electrons are relatively weakly bound to the nucleus and therefore electrons give rise to a flow of electrical current when a voltage is applied. There is no gap between the conduction (CB) and valance band (VB). If a voltage is applied to an insulator, there is no significant current measurable, because the energy gap between the VB and the CB is rather large. A semiconductor is a mixture of the two extremes. The band gap of a semiconductor is bigger then zero and up to 4 eV. At zero temperature a semiconductor would not conduct, but at higher temperature the thermal energy promotes some electrons to overcome the band gap and therefore it is conducting. [38]

The characterization of the materials is of great importance. In order to build potential NW structures to host MFs, the NW needs to fulfil certain criteria. The NW needs low disorder and high spin-orbit interaction (SOI). A desired NW would have a long coherence length and a long mean free path. A high SOI is equal to a short spin-orbit length. The distance an electron wave function retains its phase information is called the phase coherence length (l_ϕ). [38] This value is very important for quantum computing, because all the quantum states need to remain coherent during a calculation, otherwise errors will occur.

The mean free path (l) is defined as the average distance an electron travels between two scattering events. The goal is to have these numbers as big as possible to conserve the properties of the electrons. [39] Materials like InAs or InSb have a higher spin-orbit coupling because the nucleus is relatively heavy and therefore it has many protons in the nuclei, which couple to the electron spin. The spin of electrons, which are travelling through materials with high SOI, precess (Larmor precession), since they experience a relativistic effective magnetic field. [40, 41]

Let's assume to have a mesoscopic 1D system. The transport in such system can either be diffusive, ballistic or quasi-ballistic. To decide in which of those three regimes the electrons travel through the material, the comparison of the channel width (W), the channel length (L) and the mean free path (l) is important. For $L, W >> l$ the transport is in the diffusive regime. This occurs if the system has a high scattering rate. In case the mean free path is longer than the W and L ($W, L << l$) we call the transport ballistic. For $W < l < L$ we talk about quasi-ballistic transport regime. The transport of such systems is illustrated in Figure 5. [40]

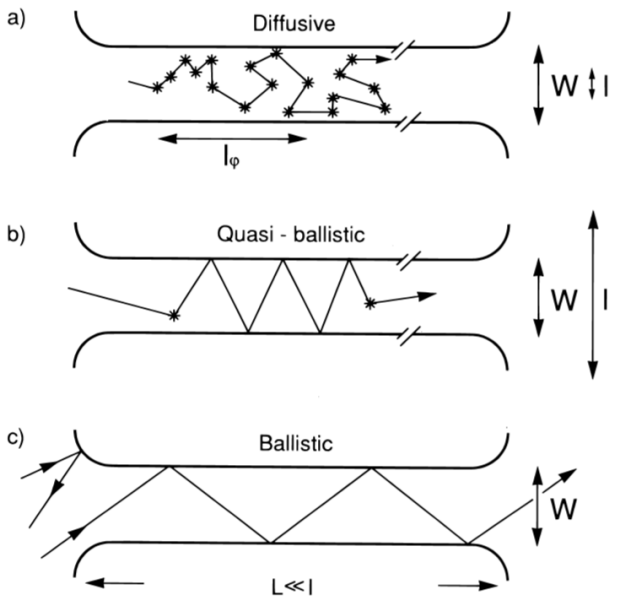


Figure 5: Illustration of the different transports. **(a)** The diffusive transport for $L, W >> l$, **(b)** quasi-ballistic transport for $W < l < L$, and **(c)** ballistic transport for $W, L << l$. Figure taken from [42].

In case of a ballistic one-dimensional system, one can tune the number of occupied modes with a voltage applied to a gate. For electrons the measured resistance of the wire increases as the voltage is decreased, due to the higher confinement. The voltage can be decreased till the wire is no longer conducting. For ballistic wires the measured resistance shows pronounced steps at $h/(2e^2 \cdot N)$, where N is an integer number. Those steps are known as quantized conduction steps. Conditions to observe such steps, next to being in the ballistic transport regime, are that the temperature is lower than the energy spacing of the modes, and the width of the channel needs to be of the order of the Fermi wavelength of the electrons. [40]

2.3.1 Fermi Wavelength

The de Broglie wavelength of electrons at the Fermi edge, is the Fermi wavelength (λ_F). λ_F only depends on the density (n), so as the electron density decreases the Fermi wavelength increases. To calculate the Fermi wavelength one can use Equation 6 [43].

$$\lambda_F = \frac{2\pi}{k_F} \tag{6}$$

If the Fermi wavelength is of the order of the length scale of the system, size quantization takes place [43].

2.3.2 Mobility

Electron mobility (μ) measures the ease with which an electron moves. It is defined as the ratio of velocity to the electric field. [44] With electric transport measurements one can extract the electron mobility. The mobility is related to the conductivity, as it is descried by Drude theory (Equation 7), where σ is the Drude conductivity, n the charge carrier density and e the elementary charge. [44] Therefore, one can estimate the quality of the system. The more impurities there are in the NW, the lower the conductivity and the mobility.

$$\mu = \frac{\sigma}{ne} \tag{7}$$

The mobility for InAs NW is lower than the mobility in bulk InAs. [45] The electron mobility also depends on the diameter of the NW. A decrease in diameter results in a decrease in mobility. [46] [47] One reason for the decrease is the influence of interface roughness scattering, which becomes more prominent as the wire diameter decreases. [48] Other reports showed that for example in Si nanowires the mobility enhances as the diameter is decreased [45], meaning that the mobility is strongly material dependent. [46]

2.3.3 Mean Free Path

In order to calculate the mean free path in the InAs NW, we need the Fermi velocity v_F and therefore the electron density n. Taking Equation 7 and reforming, we can get Equation 8, with ρ the resistivity, R the resistance, L the channel length and A the cross section area of the conducting material.

$$\sigma = \mu e n = \frac{1}{\rho} = \frac{L}{RA} \tag{8}$$

By using $\frac{1}{\rho} = GL/A$, where G is the conductance, we can rewrite Equation 8 to Equation 9.

$$n = \frac{LG}{A\mu e} \tag{9}$$

Now using Equation 10 [49], and knowing that G and n are dependent on the applied gate voltage V_g, we get Equation 11, with C the capacitance between the gate and the NW, and V_{th} the pinch-off voltage.

$$G(V_g) = \left(R_s + \frac{L^2}{\mu \cdot C(V_g - V_{th})} \right)^{-1} \tag{10}$$

$$n = \frac{C}{ALe}(V_g - V_{th}) \tag{11}$$

Next, we need the electron density at $V_g = 0$, leading to Equation 12.

$$n = \frac{C}{ALe}(-V_{th}) \tag{12}$$

V_{th} is extracted from the pinch-off measurements, C is approximated as a plate capacitor and A is estimated from images taken with the TEM (Figure 6). Now, n can be calculated for 3D. We assume that $n_{2D} = n_{3D}^{2/3}$ and $n_{1D} = n_{3D}^{1/3}$.
To calculate l we use Equation 13. Here i stands for the different dimensions which can either by 1D, 2D or 3D, and m^* is the effective mass.

$$l_i = \frac{v_{F,i}\mu m^*}{e} \tag{13}$$

If we use Equation 14 and put it into Equation 13 we get Equation 15.

$$v_{F,i} = \frac{\hbar}{m^*}k_{F,i} \tag{14}$$

$$l_i = \frac{\hbar\mu}{e}k_{F,i} \tag{15}$$

Depending on the dimension of the system the Fermi wavevector is calculated from n using different formulas. The used formulas are listed here [44]:

$$k_{F,3D} = (3\pi^2 n_{3D})^{\frac{1}{3}} \tag{16}$$

$$k_{F,2D} = (2\pi n_{2D})^{\frac{1}{2}} \tag{17}$$

$$k_{F,1D} = \frac{\pi n_{1D}}{2} \tag{18}$$

From the mean free path one can establish whether one is in the diffusive, ballistic or quasi-ballistic regime. [50]

3 Samples

Our InAs NW were grown by selective-area growth (SAG) on a (100) GaAs-based buffer layer. Reports on the promising growth of such wires were published in [51, 52, 53]. The GaAs substrate is covered with a SiO_2 mask. The mask was then patterned by using electron beam lithography (EBL). Subsequently, O_2 plasma was used to strip the resist and then the sample was etched afterwards with HF to create the mask openings, either in <110> or <100> directions. Next, the sample was loaded into the molecular beam epitaxy (MBE) cluster to grow the InAs wires. Inside the MBE a degassing step was performed to remove the native oxide on the GaAs before GaAs was grown. The GaAs does not grow on the SiO_2 layer and therefore it is possible to define by the openings, where to grow GaAs, respectively InAs. [24] Afterwards, the InAs was deposited, thereby overgrowing the defined GaAs structures, as shown in papers (see [51, 52, 53]). From one measured sample, a lamella was cut using focused ion beam (FIB) and then imaged using scanning transmission electron microscopy (STEM). With the high-angle annular dark-field imaging (HAADF), also the elementary composition is resolved, due to its sensitivity to the atomic number of atoms. [54] In Figure 6 one can see those HAADF images. From the images one can see, the shape of the pure InAs NW. Also the SiO_2 mask can be seen clearly, which defines the growth pattern.

Starting from those samples we contacted the wires with Ti/Au, deposited a dielectric and added some gates on top of the dielectric, as can be seen in Figure 6. This was done in order to fabricate a field effect transistor configuration. The gate enables application of an electric field in order to pinch-off the electric conduction of the underlying wire. In the next sections the different samples are described, the measurement results displayed, and the information gained from the results discussed.

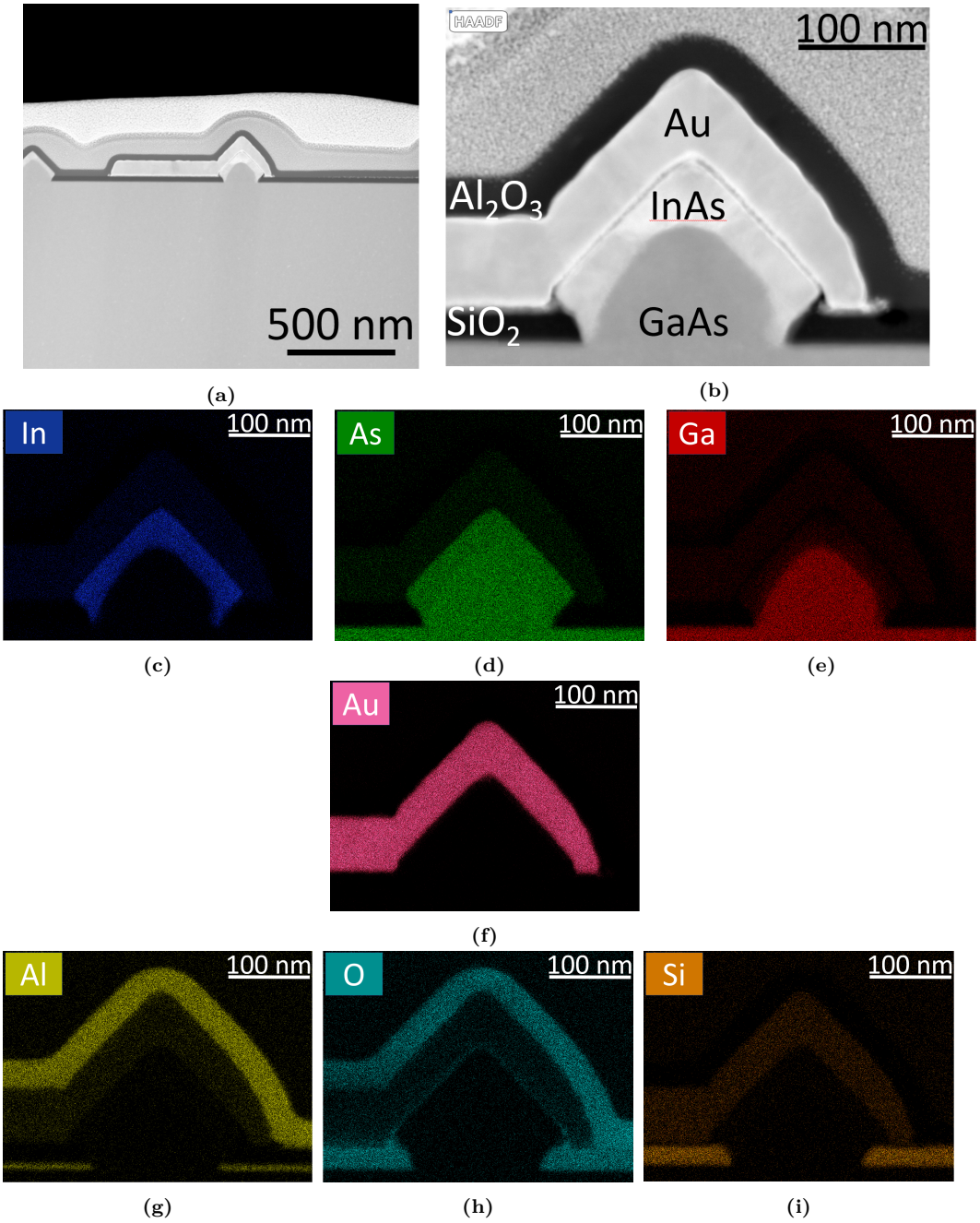


Figure 6: STEM images of a fabricated sample, taken from a lamella, cut by FIB. An overview can be seen in **(a)** and a closer view is given by **(b)**, which is a HAADF image. The material composition is displayed in **(c)** for In, **(d)** for As, **(e)** for Ga, **(f)** for Au, **(g)** for Al, **(h)** for O, and **(i)** for Si. The InAs NW, the GaAs, the SiO_2 mask, the Ti/Au contact and the Al_2O_3 dielectric can be seen from the elementary composition analysis, due to the sensitivity of the HAADF to the atomic number. Those images show that the Al_2O_3 dielectric is about 30 nm thick, the InAs NW is pure and covers the GaAs, and one can also see the SiO_2 mask, which defines where the GaAs, respectively the InAs in grown. Pictures taken by Didem Dede at Ecole polytechnique fédérale de Lausanne (EPFL).

3.1 Different Dielectrics for Gating

In order to fabricate a top gate, a dielectric is needed between the NW and the gate. For the dielectric, high-κ materials as HfO_2 and Al_2O_3 are used. The requirements for a suitable dielectric are: high dielectric constant, large effective mass for tunneling carriers, large band-gap energy, high reliability against electrical stress and compatibility with the fabrication process. HfO_2 is regarded as the most promising candidate for gate dielectrics. In addition, it is also used in commercial production. [55] Another advantage of HfO_2 is, that the native oxide on the semiconductor can be almost completely removed by using atomic layer deposition (ALD). [56] Another promising dielectric material which also is a high-κ material is Al_2O_3. [57, 58] As stated by Xu et al. [59], there are minor charge accumulations of charge carriers in the bulk of Al_2O_3 and low interface trap density between the dielectric and the semiconductor. Nevertheless, aluminium oxide has good insulation properties and a smooth interface to semiconductor materials.

We were able to grow both of these promising materials by using ALD. We first defined a window by a bilayer resist, in order to only grow the oxide in the desired area. More details about the fabrication process can be seen in Section 6.1 and the Projektarbeit. The window defined by electron beam lithography (EBL) was made, because we do not want a dielectric layer above the contact pads. The disadvantage of this method is, that the used resist starts to melt above 200 °C and the lift-off will no longer work in case the resist was exposed to higher temperatures. So, we were limited by the temperature.

According, to Suzuki et al. [60] the temperature of the ALD has an impact on the interface between the semiconductor and the oxide. They showed that lowering the temperature to about 200 °C or less does decrease the interface trap density.

In order to evaluate which oxide is suitable for our InAs NW, three samples were fabricated during the same process, to minimize variations in the fabrication. We contacted 220 nm, 140 nm and 80 nm thick wires with Ti/Au contacts, the contacts were separated by 450 nm. Then 250 oxide layers were deposited and finally a 90 nm wide gate was placed over the wire. The only difference between the samples was the materials used and the temperature during the ALD process. For the first sample we used HfO_2 and set the substrate temperature to 200 °C, for the second sample we used Al_2O_3 at 200 °C and for the third Al_2O_3 was used and deposited at 180 °C substrate temperature. The 250 layers result in a thickness of the dielectric of 40 nm for the HfO_2, respectively 30 nm for the Al_2O_3, which was extracted from the HAADF images. A representative false colored SEM image of the contacts and the gate can be seen in Figure 7.

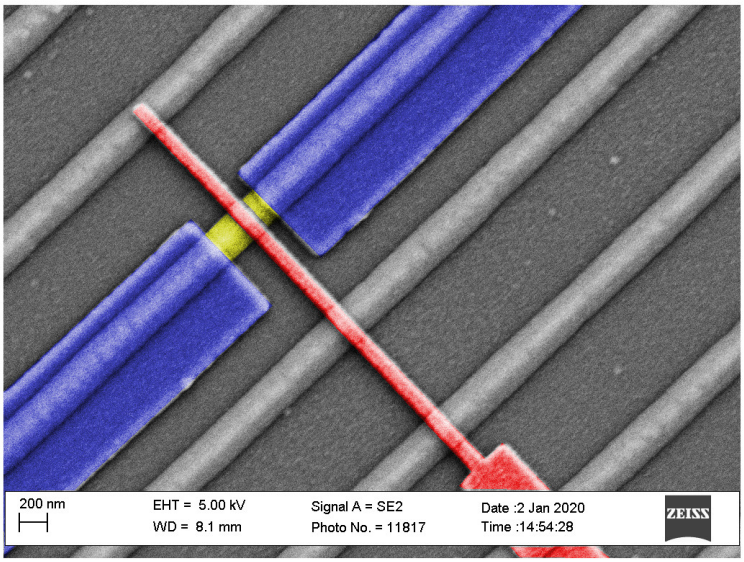


Figure 7: False-colored SEM image of the arrangement. With the 140 nm thick wires (yellow) which are contacted from the side by Ti/Au (blue). The contacts are separated by 450 nm. Above the HfO_2 dielectric layer 90 nm wide gates (red) are deposited by EBL to apply a voltage in order to pinch-off the wire.

During the fabrication we were facing some issues, which are described here to explain the changes made for the next fabrication round. We had some problems with the lift-off for the contacts. It seemed, that some structures were too close to each other. Therefore, the sample was sonicated longer, unitl we were confident with the result. The sonication process might influence the quality of the wires. For a next round, the structures should be more separated in order to have fewer problems with the lift-off and also to reduce the sonication time.

Bonding the sample was more challenging for the Al_2O_3 samples then for the HfO_2. The bonding pads for the gates were very likely to come off, when trying to bond them. This could be due to the fact, that the gate bonding pads were evaporated after the dielectric. The dielectric window step might leave some residues on the surface of the sample, which did not come off by cleaning, and so the evaporated Ti/Au gate pads did not stick well enough to the surface. Therefore, some gates could not be bonded. For the Al_2O_3 180 °C none of the gates could be bonded. Resulting in not having any pinch-off results for this sample. In order to get more statistics and also to get some pinch-off curves for all the different oxide, another round of fabricating was started.

Three differences in the fabrication process were performed. First, the design was changed,

so that the structures are more separated, this should lead to less difficulties for the lift-off. Second, the order of the ALD process for the HfO_2 was changed so that the process is started with the Hf precursor (TDMAH). This was done because in the paper of Timm et al. [56], they state that TDMAH removes the native oxide on semiconductors from the surface and one therefore gets a cleaner dielectric layer. Third, the contact pads for the gates were already written during the fabrication step of contacting the wires. This should reduce the problems with bonding the gate pads. In fact, this change in fabrication let us bond all the gates without any issues. In addition, the bigger separation of the structures resulted in a good lift-off, as expected. To change the order of using TDMAH as the first precursor did not lead to a increase in quality of the oxide, as far as we were able to tell.

3.1.1 Measurement of Different Dielectrics

All six samples were measured at 4.2 K. The measurement set up is displayed in Figure 8. An AC voltage from a lock-in and a DC voltage from the digital-to-analog converter (DAC) are applied to the sample. The SD-Box combines the two signals, before the sample. Then after the sample, the current is transformed into a voltage using an I/V converter. This voltage is then measured by a lock-in (AC) and a DMM (DC). With the voltage probes, the applied voltage was measured and amplified by a pre-amplifier. To apply a voltage to the gate, the DAC is used and a ground decoupler in order to reduce the noise. Then for calculating the resistance or conductance we use only the signals from the lock-ins, so only the AC part.

For all the wires, first the conductance was measured by sweeping the source drain voltage from -1 to 1 mV. A representative measurement can be seen in Figure 9.

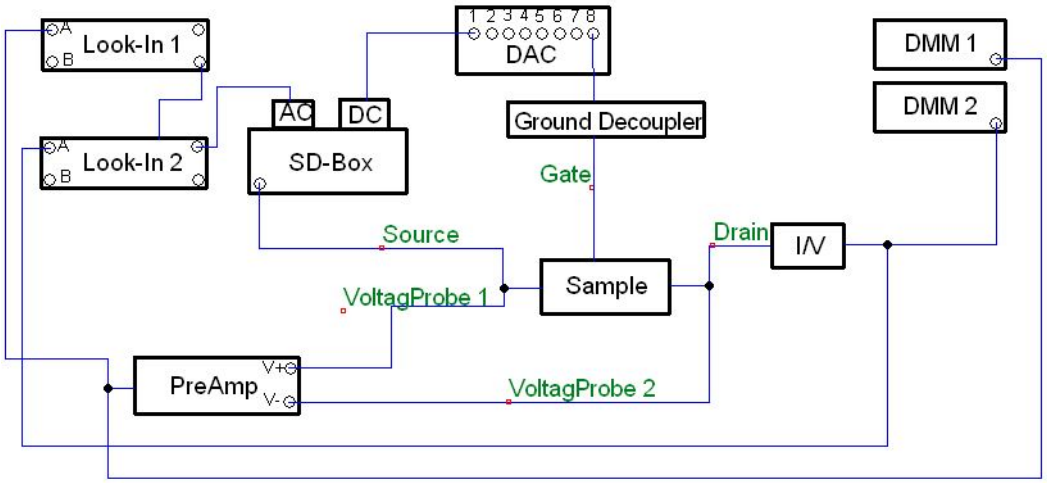


Figure 8: A schematic of the used measurement set up. The lock-in, DMM and the DAC were connected to a computer to read out the measurements and to set parameters, as for example the voltage applied to the source drain.

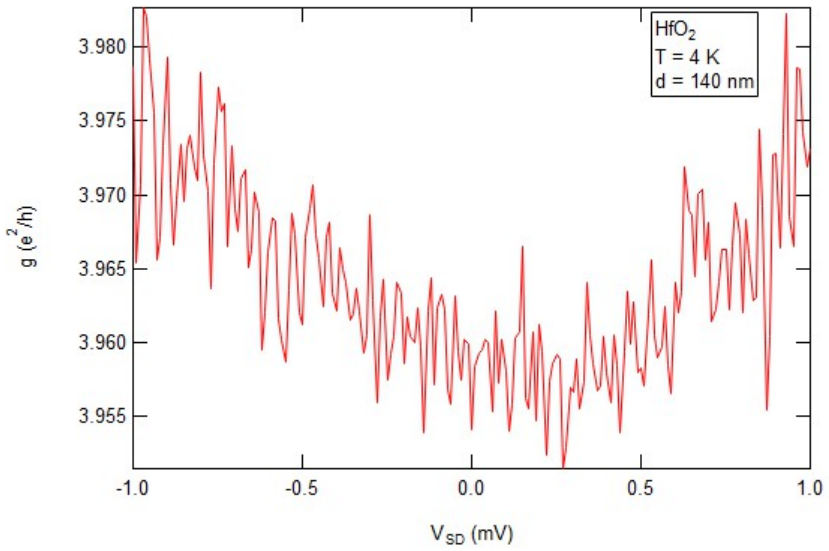
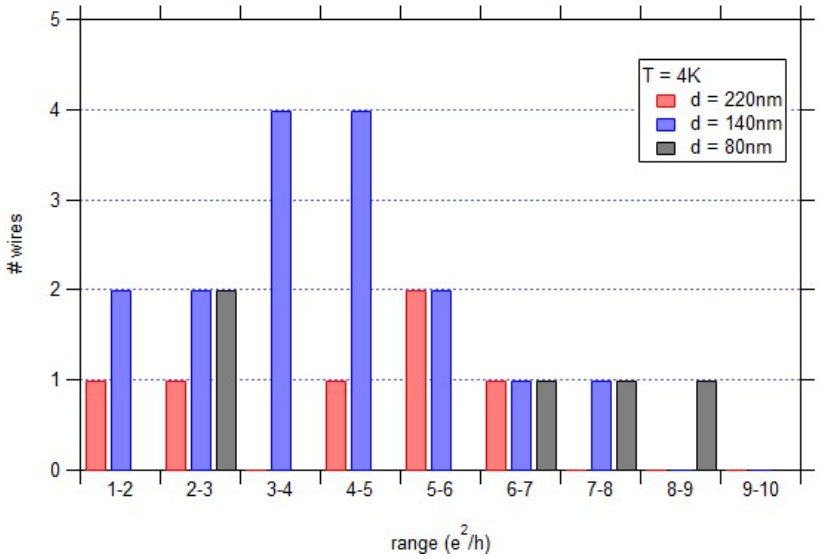


Figure 9: A representative measurement of the conductance, while sweeping the source drain voltage from -1 to 1 mV of a 140 nm thick NW.

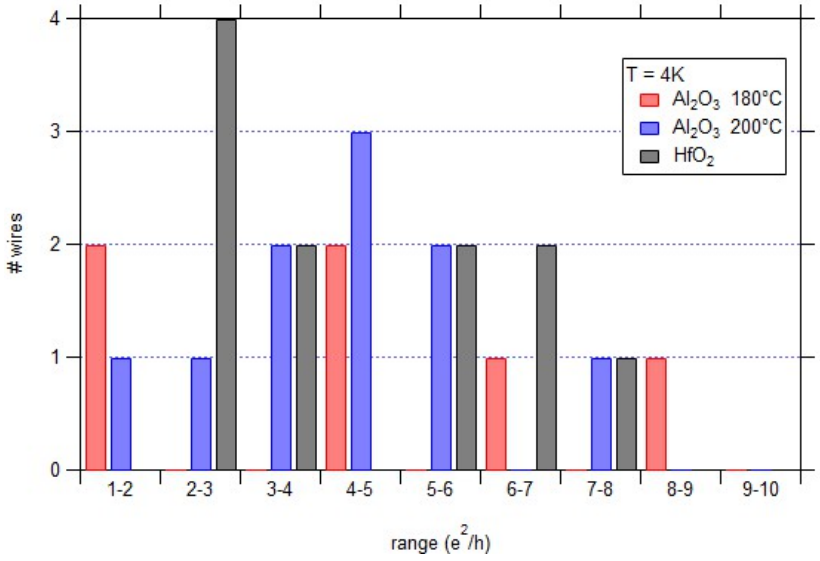
In the following, for the conductance of the wire, the measured conductance at zero bias and no applied gate voltage is compared. For the depicted measurement of the 140 nm thick wire in Figure 9 the conduction value is $3.96\,e^2/h$. To display the results, histograms were made with a range of e^2/h (Figure 10). One histogram shows the result separated by the defined NW width's and the second one has the results separated by the oxide.

In total there were 27 wires conducting above one e^2/h. From the histogram one can see

that most of the working wires were 140 nm thick ones, but the highest conductance was measured for a 80 nm NW. From the histogram separated by the oxide no tendency can be seen. This was expected since the dielectric should only minimally influence the conductance of the wire.



(a)



(b)

Figure 10: The histogram shows the number of wires conducting in a certain range. The results are separated by the defined NW width's **(a)**, respectively **(b)** by the oxide.

To get an idea of the quality of the dielectric, a negative voltage was applied to the gate in order to pinch-off the current flow through the wire. A suitable dielectric would then show

reproducible measurements. Also the pinch-off voltage (V_{th}) would be ideally independent of the sweep direction of the gate and the hysteresis shall be as small as possible. The difference in pinch-off voltage (ΔV_{th}) for sweeping the gate voltage from negative to positive or vica versa is shown in Figure 11 for the different oxides. HfO_2 shows in general less hysteresis, except for one wire which had a ΔV_{th} way bigger then all of the others. In addition to the smaller ΔV_{th}, the fabrication with the HfO_2 gave the highest yield and worked with the least difficulties. Those results suggest to continue using HfO_2 as the dielectric.

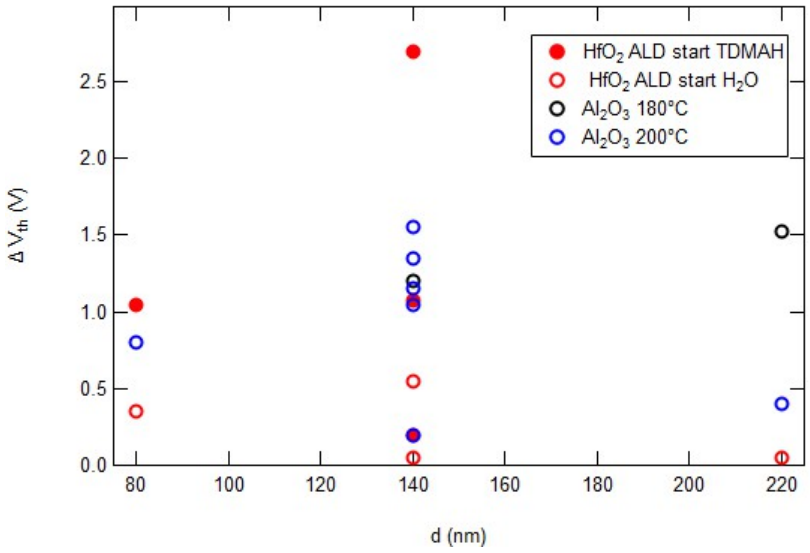


Figure 11: The difference in the pinch-off voltage (ΔV) is plotted against the width of the wires for the different oxides. For all oxides there were 250 layer deposited and the contacts are separated by 450 nm. The gate has a width of approximately 90 nm. The two HfO_2 devices have one difference in fabrication. One of the oxide was deposited starting with the hafnium precursor (TDMAH) and the other was started with water as the first precursor. Therefore, the results for the HfO_2 are labelled separately.

By assuming a mobility independent of the gate voltage, we used the same model as Gül et al. [49] and Ford et al. [46] (Equation 10). For the capacitance C we assumed a plate capacitor. The dielectric constants used are $\epsilon_{Al2O3} = 9.5$ [61] and $\epsilon_{HfO2} = 6.5$. [53] With this model we were able to extract the mobility from the pinch-off curves, in order to get an idea about the quality of the wires.

A representative pinch-off curve and the fit (Equation 10) to extract the mobility can be seen in Figure 12.

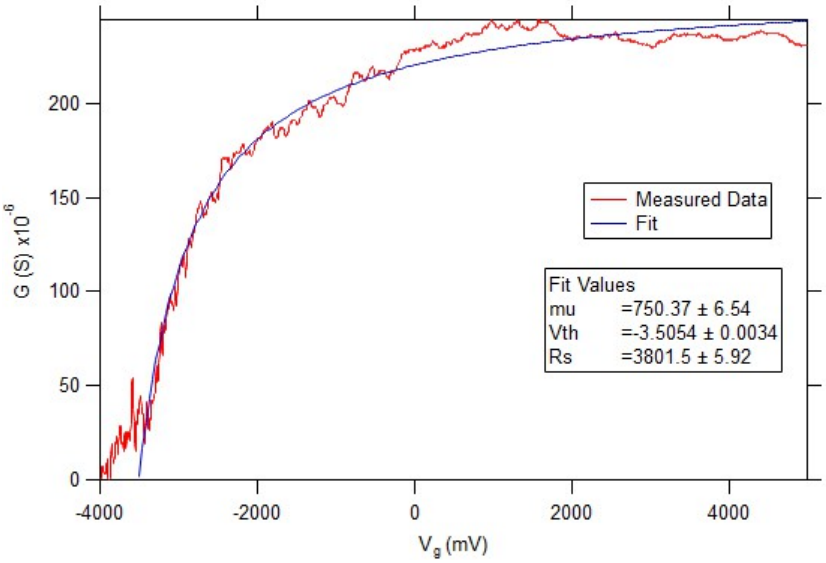


Figure 12: A representative measurement result of the conductance, while reducing the gate voltage till the wire is pinched. By using Equation 10 the mobility is extracted. For the capacitance C it is assumed that we have a plate capacitor and L is the width of the used gate to pinch the wire. Rs is the resistance extracted by the fit for the measurement set up and μ is the mobility which is here about $750\,\mathrm{cm}^2/\mathrm{Vs}$.

The minimum (μ_{min}), the maximum (μ_{max}) and the mean extracted mobilities (μ_{mean}) are shown in the following table. For each wire two measurements sweeping from positive to negative and two from negative to positive gate voltage were taken. This results in four pinch-off curves per wire. For each measurement a mobility was extracted. From those the average is taken and set to be the mobility of the wire, the maximum and the minimum extracted mobility for the wires are listed in Table 2. Then for the μ_{mean} the average of all extracted mobilities for a specific oxide is taken. For Al_2O_3 180 °C two wires were working, for Al_2O_3 200 °C seven wires were working and for HfO_2 200 °C eight wires were working. The error for the mobilities is calculated using the standard deviation.

Dielectric	μ_{min} [$\mathrm{cm}^2/\mathrm{Vs}$]	μ_{max} [$\mathrm{cm}^2/\mathrm{Vs}$]	μ_{mean} [$\mathrm{cm}^2/\mathrm{Vs}$]
Al_2O_3 180 °C	380 ± 70	860 ± 210	620 ± 280
Al_2O_3 200 °C	130 ± 20	1040 ± 60	580 ± 275
HfO_2 200 °C	250 ± 10	1190 ± 170	700 ± 350

Table 2: The extracted values for the mobility using Equation 10. The error for the mobilities are calculated using the standard deviation. There were four pinch-off curves measured and for each a mobility was extracted. From those the average is taken and displayed in the μ_{min} and μ_{max}. Then for the μ_{mean} the average of all extracted mobilities for on oxide is taken. For Al_2O_3 180 °C two wires were working, for Al_2O_3 200 °C seven wires were working and for HfO_2 200 °C eight wires were working.

Due to the low statistic of Al_2O_3 180 °C with only two wires pinching-off, no conclusion regarding the mobility, can be made for this dielectric.

From Equation 7 one can see that the mobility is proportional to the conductance. This was also seen in our results. To visualize this, the conductance is plotted against the extracted mobility. The graph can be seen in Figure 13.

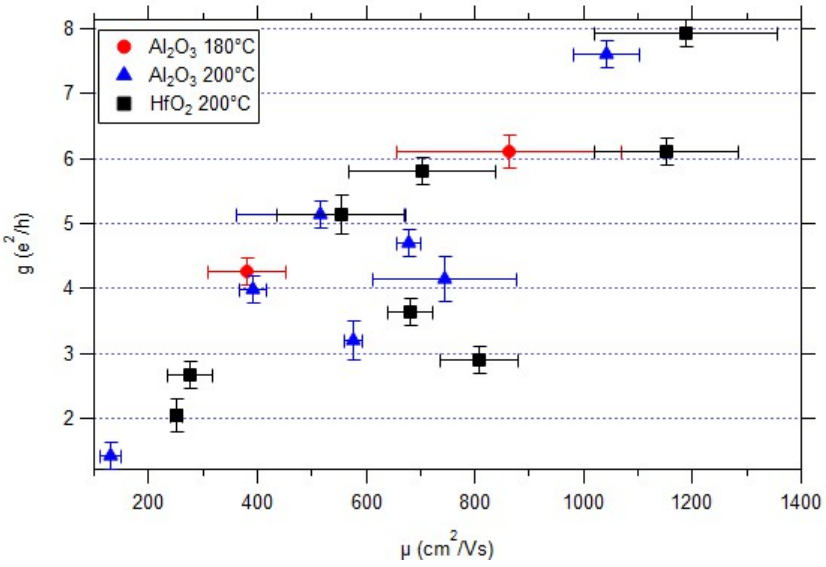


Figure 13: The conductance is plotted against the extracted mobility. One can see as expected from Equation 7, the linear dependence of the mobility to the conductance.

The extracted mobilities showed no clear difference, which oxide to choose, but it suggests HfO_2 due to the highest mean for the mobility. Nevertheless, it is also possible that the differences in mobility are more influenced by the nanowire growth than by the oxide, which cannot be ruled out. Although the wires were all grown on the same sample at the same time. The fabrication process for the HfO_2 was the most reliable in turns of a working lift-off process. The HfO_2 also showed in general the least hysteresis in the pinch-off curves and the extracted mobility seems to be a bit higher than the one of the Al_2O_3. Therefore, it was concluded that HfO_2 is the most promising candidate to continue fabricating other devices. Ford et al. [46] used the vapor-liquid-solid (VLS) method to grow their InAs NW. They showed mobilities of 2'500, 4'000 and 6'000 cm^2/Vs for NW with a diameter of 15, 25 and 35 nm at room temperature (RT) and at temperatures of 50 K they showed mobilities of 10'000 to 16'000 cm^2/Vs. Similar values for VLS grown InAs NW are also observed at 4.2 K by Schroer and Petta [62]. This shows that the quality of our SAG NW regarding the mobility is lower than the one which can be produced by VLS. The disadvantage of using

VLS is that only a limited number of interconnections between the wires can be grown and that the NW need to be transferred after growth. Therefore, the VLS method lacks at its scalability. [51]

Next, we calculated the density and the mean free path from the pinch-off curves by using the equations shown in Section 2.3.3. Overall, the measured data we extracted, yields an average n_{3D} of $(1.2 \pm 1)10^{24}\,\frac{1}{\mathrm{m}^2}$ and for n_{1D} of $(1.2 \pm 0.3)10^{8}\,\frac{1}{\mathrm{m}}$. For the mean free path we extracted values of $l_{3D} = 16 \pm 9\,\mathrm{nm}$ and $l_{1D} = 8 \pm 5\,\mathrm{nm}$. In the paper of Roulleau et al. [63] they state that the mean free path in InAs NW is about 30 nm and Hansen et al. [64] state that l is about 60 to 100 nm. It must be said that our measurements were done at 4.2 K and at atmospheric pressure. It is shown in the paper of Gül et al. [49] that in a vacuum the mobility and therefore also the mean free path tend to increase.

Subsequently, the λ_F was calculated using Equation 6. The results is $\lambda_{F,1D} = 36 \pm 11\,\mathrm{nm}$. From those numbers, we conclude that we are not in a one-dimensional regime. It is more likely that due to the large dimensions of the NW (>80 nm) compared to the Fermi wavelength, the system is in the 3D regime.

In Hansen et al. [64] they say in addition, that for gates $< 100\,\mathrm{nm}$ one can see signs of quantized conduction and therefore the mean free path is of the order of the gate width. In Section 3.1.2 it will be discussed, that we also see signs of quantized conduction. This leads to the assumption, that our mean free path also is of the order of the gate, which would be of about 90 nm. The values observed by the calculations of l via the mobility are about 9 times smaller. Reducing the gate should give a clearer picture about the mean free path. This is because if we would then see ballistic transport, we could conclude, that the used gate is of the order of l. In the case, that we do not see ballistic transport behavior, we can conclude that l is smaller than 90 nm.

3.1.2 Testing for Ballistic Transport

As mentioned in the section above, while processing the data in order to extract the mobility, we observed in most pinch-off curves a signature of plateaus around $2\,\mathrm{e}^2/\mathrm{h}$ (see Figure 14). The plateaus are like the ones seen by Aseev et al. [65] and can be seen in the following figure.

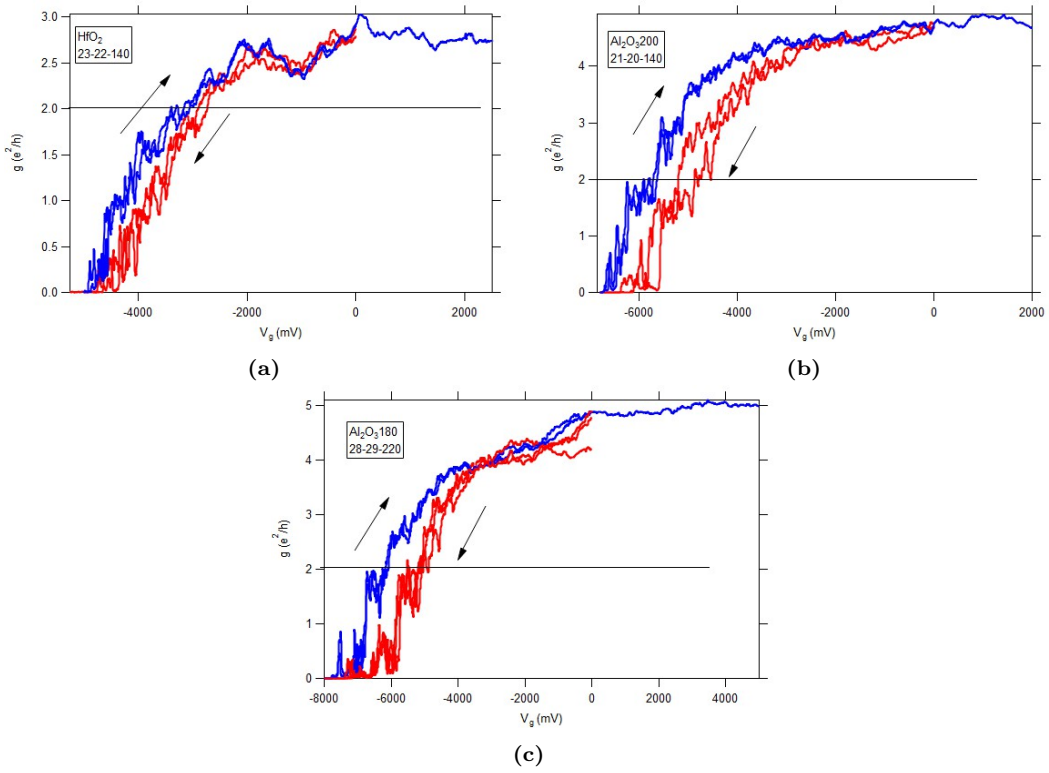
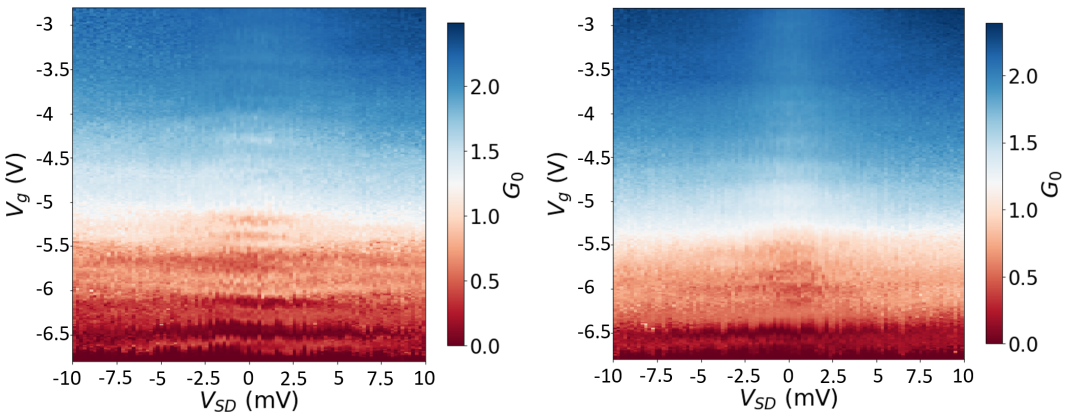


Figure 14: Representative pinch-off curves for the HfO_2 **(a)**, the AlO_2 200 °C **(b)**, and the AlO_2 180 °C **(c)** samples. The arrows indicate the direction of sweep, the red curves are the sweeps from positive to negative voltage and the blue ones are vica versa. The black horizontal line helps to see the plateau around $2\,e^2/h$, which might be due to quantized conductance.

In order to clarify if we see quantized conduction and therefore would have ballistic transport, we did bias spectroscopy measurements. Therefore, the gate voltage was swept at different bias voltages.

In case of ballistic transport, the conductance will only be quantized at finite bias voltage if the chemical potential of the source and the drain occupy the same sub-band. This results in diamond shaped regions in a bias spectroscopy measurement. From the diamonds one could also gain information about the sub-band spacing of the measured InAs NW. [65, 66, 67, 68] In addition, we also measured bias spectroscopy at different magnetic fields ranging from 0 to 8 T in steps of 2 T. A representative result for the bias spectroscopy at zero field and at 8 T can be seen in Figure 15. Also, we measured zero bias conductance while varying the top gate and the magnetic field. The result of the measurements is displayed in Figure 16.



(a) **(b)**

Figure 15: Bias spectroscopy of a 220 nm thick wire, of the Al_2O_3 sample. The color scale on the right is in units of $2\,e^2/h$. The same measurement was done at zero field **(a)** and at 8 T magnetic field **(b)**. The magnetic field is applied perpendicular to the sample plane. There is no significant difference between those two measurements. These results indicate that there is no ballistic transport due to the absence of diamonds.

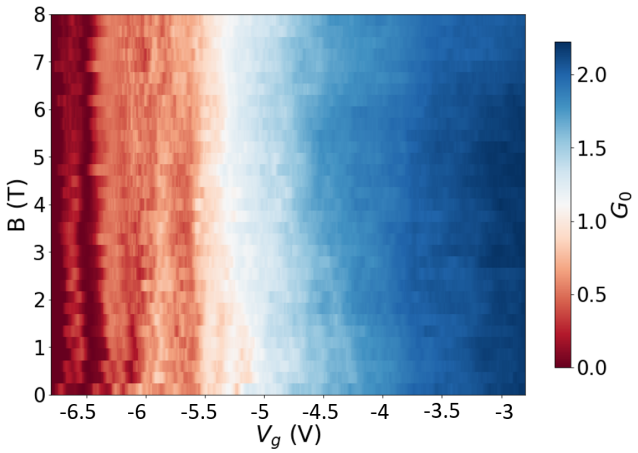


Figure 16: Zero bias conductance measurement of a 220 nm thick wire, of the Al_2O_3 sample, while varying the magnetic field and the top gate. The magnetic field is applied perpendicular to the sample plane. The color scale on the right is in units of $2\,e^2/h$. Also, this measurement indicates that there is no ballistic transport.

The results do not show a magnetic field dependence, nor do they show diamonds in the bias spectroscopy. Therefore, it was concluded, that we do not see ballistic transport. The plateau like behavior which we see at $2\,e^2/h$ is probably due to impurities in the wires.

3.2 Optimizing Conditions to Measure Ballistic Transport

Due to the fact, that most of the wires were conducting above $2\,e^2/h$, we decided to test smaller wires with defined width's of 20, 35, and 50 nm. In addition, we did some dose tests to reduce the width of the gate down to 60 nm and also to decrease the distance between the contacts to 400, 300, 200 and 100 nm.

In the paper of Byoung Hun Lee et al. [69], they showed that they can do thin HfO_2 dielectrics, which are still not leaking. We produced three samples with a field effect transistor configuration, varying the number of HfO_2 layers deposited. We deposited 200 layers of HfO_2 for the first sample, 150 layers for the second and 100 layers for the third. This gave us a bigger lever arm to gate the wire. Also, it was hoped that the thinner oxide is going to reduce the hysteresis for the pinch-off curves, which was confirmed by the measurement of the device. On all the samples we were able to pinch the wires off, without having severe leakage ($<$50 pA) from the gate to the wire.

Some gates were not fabricated. For the 100 layer sample all gates were working, for the 150 layer about half of the gates, and for the 200 layer most gates did not work. Imaging with the SEM revealed that part of the 60 nm gates were not written or miss aligned, although the dose test gave good looking gates. The reason why we had problems on the actual sample, was probably due to the fact that the dose test was performed on a chip without the dielectric deposited. This assumption is reinforced by the fact, that the gate fabrication on the thinner HfO_2, resulted in less failure.

Because of the few gates working on the 200 layer chip, it was decided to redo the step of fabricating gates on these same samples. This time the 90 nm gates were used if there was no gate written at all. Then if there was already a gate there, which did no work or was misaligned, we fabricated a gate over the whole NW channel.

Again, we did measurements at 4.2 K and started with measuring the conductance while sweeping the source drain voltage from -1 to 1 mV, followed by applying voltage to the gates in order to pinch the electrical current through the wire. As for the sample described in Section 3.1, also for those samples we saw step-like behavior around the conductance quantum G_0. Hence, we did bias spectroscopy and observed the results displayed in Figure 17 for (a) the 150 layer sample, measuring a 35 nm wide wire with a 60 nm gate.

In contrast to the before seen bias spectroscopy, here signs of diamonds were observed in the measurement results. Those might occur due to ballistic transport or to disorder in the wire.

A similar result was observed for the 200 layer sample, where a 50 nm thick NW with a

60 nm gate was measured. More clear diamonds were seen on the same sample, when we measured a 35 nm thick and 200 nm long NW, with a gate covering the whole wire. The measurement result can be seen in Figure 17. The data was post processed, because the voltage drop across the contact resistance and the wiring of the setup was taken into account. Due to the mobility fit, we assumed to have a resistance, occurring from the used wire, and the imperfect contacting between the NW and the fabricated contacts, of about 4 kΩ. This resistance was used to renormalize the results in Figure 17.

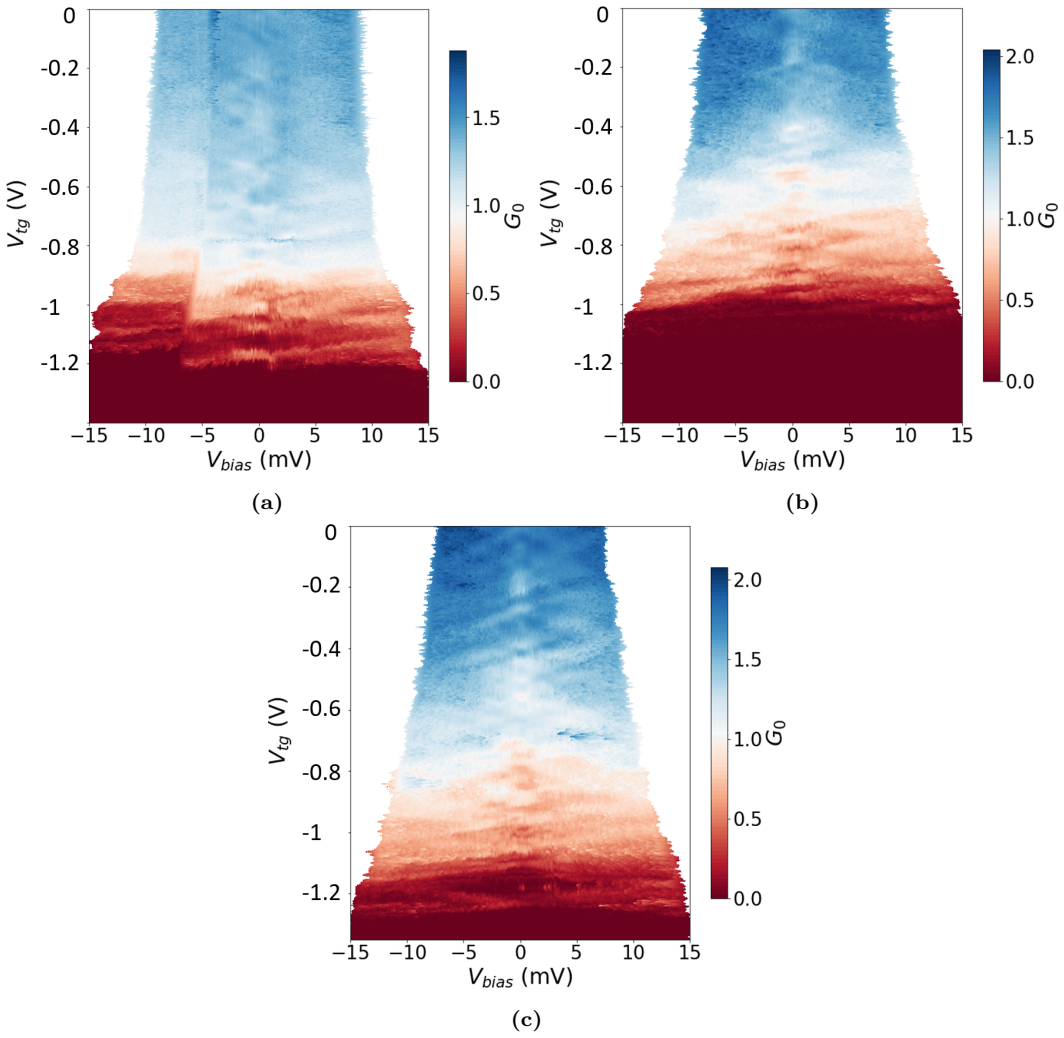


Figure 17: Bias spectroscopy measurements for different NW renormalized. **(a)** Measurement result of the 150 layer sample measuring a 35 nm wire of distance 300 nm and a 60 nm gate. In the data there can be seen a charge switcher. **(b)** the 200 layer sample measuring a 50 nm wire of distance 200 nm and a 60 nm gate, and **(c)** the 200 layer sample measuring a 35 nm wire of distance 200 nm and a gate above the full length of the wire. Here in (c) the diamonds can be seen the clearest.

For the 35 nm thick wire with 200 layers of HfO_2, we also extracted the mobility as described in Section 3.1 with Equation 10. Using the mobility the mean free path, the electron density and the Fermi wavelength was calculated and is displayed in Table 3.

	1D	**2D**
μ	5'400 $\pm$ 100 cm^2/Vs	
l	46 $\pm$ 4 nm	73 $\pm$ 6 nm
n	(8 $\pm$ 0.02) 10^{15} $\frac{1}{m^2}$	(9 $\pm$ 0.01) 10^7 $\frac{1}{m}$
λ_F	45 $\pm$ 1 nm	28 $\pm$ 1 nm

Table 3: For the 35 nm wide NW with 200 layers of HfO_2 the mobility was extracted as described in Section 3.1. In addition, the mean free path, the electron density and the Fermi wavelength was calculated for the case of a 1D, respectively a 2D wire.

Comparing the Fermi wavelength to the size of the channel suggests size quantization. The width and the height of the wire are probably of the same size as the Fermi wavelength. This results in the conclusion that the system can be seen as one dimensional or quasi-1D.

At this point it is not clear if the diamonds seen in Figure 17c are due to quantized conduction, because of the irregularity of the diamonds. The irregularity suggests the presence of several dots with different sizes located somewhere under the gate. Nevertheless, the fact that plateaus at $2\,e^2/h$ are seen points towards quantized conduction. As diamonds seen in Figure 17c, which are possible signs of quantized conduction, suggested due to Hansen et al. [64], that l is in the order of the gated channel, which is in this case 200 nm. Comparing this with the value calculated for l one can see, that the two numbers do not agree by more than a factor of two.

One possible source of error in the calculation is, that it is assumed to have a plate capacitor. The capacitance influences the fit and therefore the mean free path. Looking at the STEM picture it can be seen that the assumption of a plate capacitor is not perfectly true. Maybe this assumption does not hold. Then the exact geometry of the thinner defined wires is not known, due to the lack of a STEM image of those wires. So the hight and the width of the wire might not be estimated precisely.

By measuring the device at different magnetic fields, it would reveal if quantized conduction is seen and therefore if the electron transport is in the ballistic regime. In case, that all of the promising wires, including the ones with the 60 nm gate, do not show signs of ballistic transport, it would be assumed that l is smaller than 60 nm. Otherwise, if more arguments for ballistic transport are measured, l is at least of the size of the used gate. Due to the lack

of time and capacity of cryostat's, which can apply a magnetic field, the promising wires could not be measured at magnetic field, within the time frame of this work.

3.3 Fabrication of Five Gate Device

Due to the promising results shown in Section 3.2, the goal was to fabricate more than one gate. This would increase the possibility to manipulate the electron wave function. For example, one could try to measure quantum dots. Therefore, a dose test was started, where the recipe for fabricating the gates was strongly changed. On our test chip we had 44 nm thick wires defined, which is close to the NW width, on the device we want to fabricate.
First another resist was used, we used PMMA 1.8% and spun it at 6'000 rpm for 45 s. This step was done twice. This should lead to a thin PMMA layer, which is important to be able to write small gates very close to each other. On the other hand the resist has to be thick enough that also the NW are completely covered with resist, otherwise lift-off probles occur as can be seen in Figure 18. Then five single pixel lines were written in 60, 75, 100 and 150 nm separation to each other with the SEM. For the development, the same developer as for the other samples was used, but the developer was cooled with dry ice to $-18.5\,^{\circ}\mathrm{C}$ and the sample was put in the cooled developer for 30 s. Then the device was blow dried for about a minute with N_2. To eliminate occasional breaks in the gates as can be seen in Figure 19, no more reactive ion etching (RIE) was done. Afterwards, 1 nm of Ti and 9 nm of Pd were evaporated. The lift-off was done in acetone (ACE) over night at $50\,^{\circ}\mathrm{C}$.
At the end gates shown in Figure 20a resulted, which shows lines without breaks and good geometries. Only the 60 nm separated lines (on the left in the SEM image in Figure 20a) did not work. The resulting width of the gate is about 30 nm and the minimum spacing is 40 nm. This was measured using the SEM, the image can be seen in Figure 20b. The exact recipe is listed in Section 6.3.

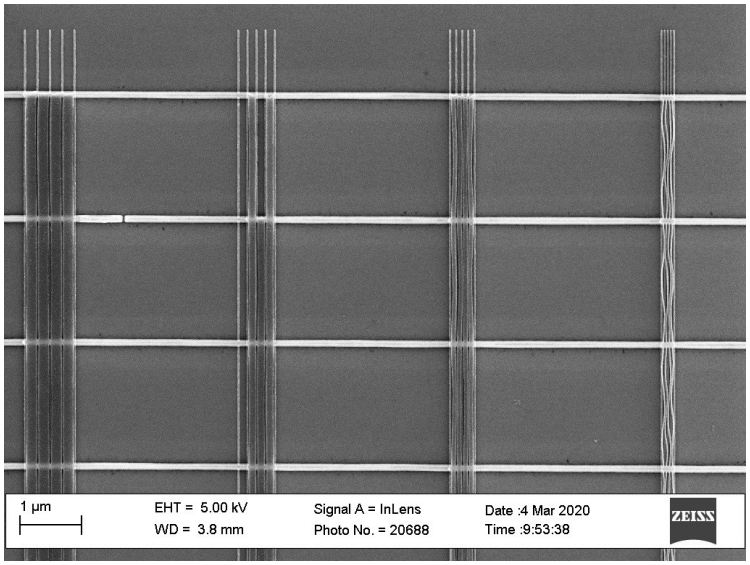


Figure 18: SEM image taken with the InLense. One can see that the lift-off did not work properly, due to too much exposure on the InAs wires, where the resist is assumed to be thinner then above the SiO_2 mask.

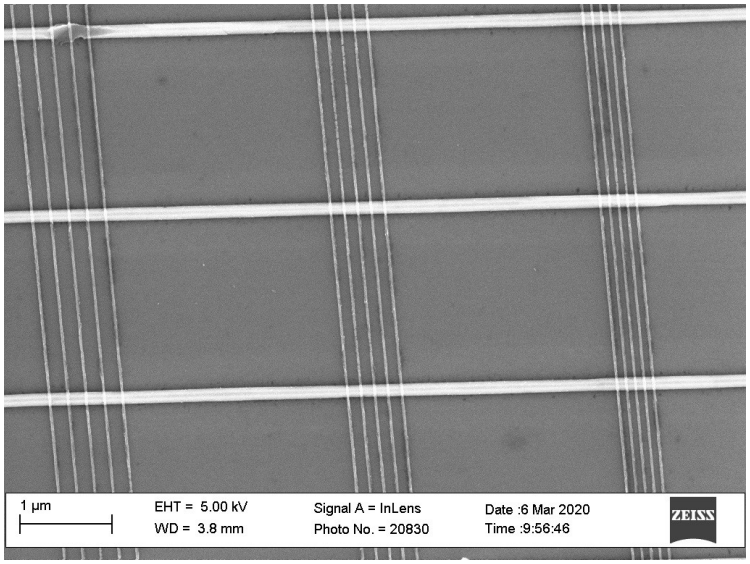
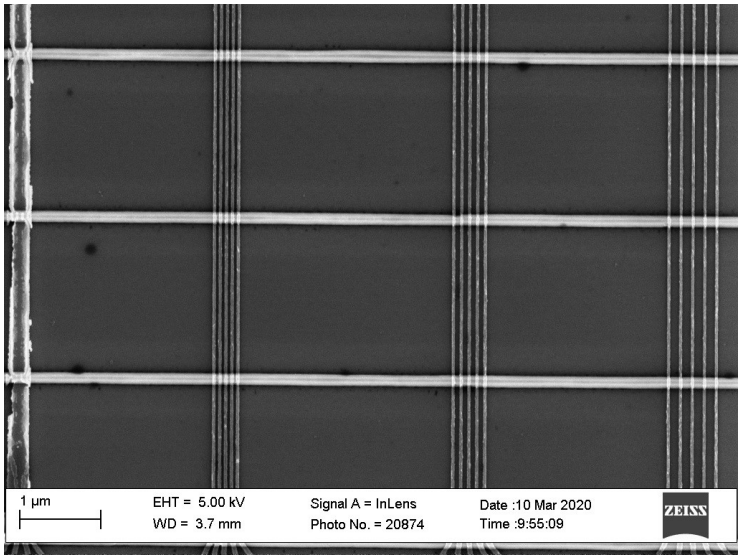
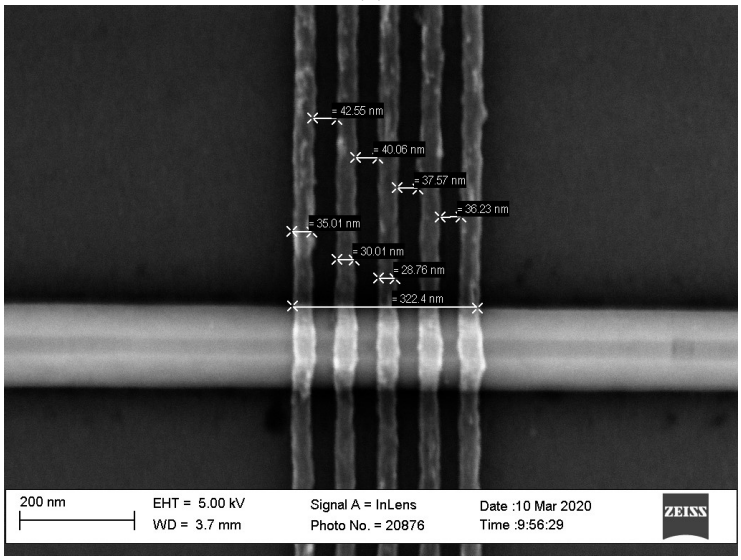


Figure 19: SEM image taken with the InLense. One can see that the lift-off did work, and the gates are separated also on the wire. With still occasional breaks in the wire, which indicated that we do not have the proper dose, yet.



(a)



(b)

Figure 20: SEM image taken with the InLense. **(a)** An overview of the gates. One can see that the five gate lines are well formed for the separation of 75, 100 and 150 nm. On the left the separation of 60 nm did not work. **(b)** A zoom in on the 75 nm separation wires. From the measurement one can see that the gates are about 30 nm wide and have a spacing in between of about 40 nm.

Next, it was tried to use those gates, to fabricate a similar device as in Section 3.2, just the contact spacing was fixed to 450 nm and the five 30 nm gates were fabricated on top of the 100 layers of HfO_2. The fabrication of this device could not been finished, due to the extraordinary situation regarding Covid-19.

4 Conclusion & Outlook

Investigating whether to use HfO_2 or Al_2O_3 as a dielectric for our SAG InAs NW, was done by fabricating a field effect transistor configuration. The wires were 220, 140 and 80 nm thick, the gate was 90 nm thick and for each oxide the number of deposited layers was the same. First, the conductance was measured at 4.2 K, followed by a pinch-off measurement. The results suggest to use HfO_2, due to the lower hysteresis in the pinch-off curves and the more reliable fabrication process. The extracted mobility using the model of Gül et al. [49], did not show a clear difference between the oxides. The extracted mobilities are in general lower than the ones shown in other papers for InAs NW grown by VLS method (see [46, 62]). The advantage of the wires used in this work is that they are grown by SAG, which is a scalable process.

Further, the charge carrier density, the mean free path and the Fermi wavelength were extracted using the pinch-off curves. To check the extracted densities and mobilities in an idependent experiment, one should construct hall measurements on the wide 220 and 140 nm wires. This would make it possible to extract the electron density in a more direct way. The comparison of the values extracted in this work and the values via the hall measurement should give an idea about the truth of the values. In addition, this should give a hint if the used model holds for the measured devices.

Then, in the pinch-off curves of the samples with different oxides, plateaus around $2\,e^2/h$ were seen. Considering that from the measurement results one needs to subtract the contact resistance, the plateaus occur at around $3\,e^2/h$. The possibility that those were quantized conduction plateaus was denied by the results of bias spectroscopy at different magnetic fields, a magnetic field against gate voltage sweep, and the comparison of the extracted values of λ_F to the sizes of the wires. Meaning that we do not see ballistic transport and are not in a one-dimensional regime.

Next, the conditions were adapted to try to be in a one-dimensional regime and thereby increasing the probability of measuring ballistic transport. This was done by using thinner InAs nanowires of size 20, 35, and 50 nm, reducing the gate width to 60 nm, and decreasing the number of HfO_2 layers deposited. Due to some issues with fabrication, gates covering the whole channel length of 200 nm were also fabricated.

The measurements at 4.2 K showed no leakage of the approximately 14 nm thick HfO_2. From the pinch-off curves mobilities up to 5'400 cm^2/Vs are extracted. The calculated λ_F is of the order of the width and the height of the NW, which suggests a one-dimensional regime.

Again, plateaus at $2\,e^2/h$ were observed in the pinch-off curves. This time also the bias spectroscopy at zero magnetic field shows possible signs of ballistic transport. To make a stronger statement about if ballistic transport is seen, further devices have to be made and measurements need to be performed at different magnetic fields.

From the promising results it would be interesting to construct a device with more than one gate over the InAs NW. Therefore, several dose tests were made, which resulted in fabrication of five gates of the width 30 nm separated by 40 nm. If such gates can also be fabricated on an actual device, there we are optimistic that ballistic transport can be measured. To confirm the ballistic transport of the wire one should be able to show that the resistance of the wire defined by one gate is the same as the one measured across two (or more) gates, as long as the total length of the measured wire is smaller than the mean free path. In addition, one can try to make quantum dots, and other very interesting measurements can be performed.

With the indication to see ballistic transport in the SAG NW, next one should try to fabricate a superconducting material in proximity to the NW. Therefore, one needs to establish a fabrication recipe in order to place the superconducting material on the templated InAs NW. This would lead to the possibility to study the transport in a superconductor-semiconductor-superconductor junction. In addition, by applying a magnetic field to the system one could drive the system into the topological superconducting phase. Andreev reflection processes might be measured and perhaps even signatures of MZMs. [5, 31, 70, 71] This should result in getting one step closer to a topological qubit. To realize the vision of building a fault tolerant quantum computer.

5 Acknowledgement

A big thank goes to Prof. Dr. Dominik Zumbühl for giving the opportunity to do the master thesis in his group, taking the time to discuss the results, and for supervising. Then a special thank goes to Kris Cerveny, for supervising me, taking the time to explain lots of things, showing me how to fabricate devices, and also how to measure them, and post process the data. Further, I want to thank Dr. Taras Palatiuk and Dr. Mohammad Samani for always helping me and giving advice for the measurement set up and the data processing. Dr. Martin Friedl and Didem Dede also deserve a special mention. They grew and provided the SAG NW and took the time to make the STEM images. Miguel J. Carballido showed and helped to fabricate the five gates: Also, a thank you goes to the whole Zumbühl group for the help, always taking time to answer questions and creating a excellent laboratory and office environment. It was a pleasure to work with all of you. Last, I would also like to thank Nicolas Forrer and Rahel Kaiser for proofreading the manuscript and supporting me and also a big thank goes to my family for supporting me and paving the way for me to have such an education.

6 Fabrication Recipe

6.1 Samples for Different Dielectrics for Gating

Here the fabrication recipe for the samples described in Section 3.1 is listed.

6.1.1 Prepare Resist

1. Cleaning
   - 5 min in ACE.
   - 5 min in isopropanol (IPA).
   - Blow dry with N_2.
   - Put on hot plate 2 min at 120 °C.
2. Spinning Polymethylmethacrylat (PMMA)
   - Spin 4.5% PMMA (4'000 rpm, step size 4, 40 s).
   - Bake for 7 min at 180 °C.
   - Add 50 nm Au particles with a toothpick in each corner of the sample.
   - Check under light microscope the resist for even coating and measure the distances from the edges to the Au puddles and the tungsten alignment markers.

6.1.2 Electron Beam Lithography of Contacts & Development

3. Electron Beam Lithography (EBL)
   - Prepare GDS files for writing the contacts, the contacts are defined to be separated by 500 nm which results in a separation of 450 nm.
   - Put sample into SEM, set up focus, angle correction and do alignments on the tungsten markers.
   - Do EBL with 30 kV, dose 200 μC/cm^2 and aperture 120 μm for 2 mm field, respectively 30 kV, dose 200 μC/cm^2 and aperture 10 μm for 400 μm field.
4. Development
   - Put sample into developer ((MIBK + IPA) : MEK, ration 100:1.3) for 90 s at 4 °C.
   - 30 s IPA.
   - Blow dry with N_2.

6.1.3 Reactive Ion Etching

5. Reactive Ion Etching (RIE)

   - Use RIE to get rid of PMMA residues in the defined channels (16% O_2, 5×10^{-5} mbar, 30 W, 1 min, 250 mTorr).

6.1.4 Ammonium Polysulfide Etching & Evaporation of Ti/Au

6. NH_4S_x- Etching

   - Prepare two beakers (250 ml) with deionized (DI) water.
   - Stir NH_4S_x solution for at least 20 min using magnetic stirrer.
   - Prepare a beaker (20 ml) with 10 ml DI water and put it on the hot plate at 40 °C for at least 20 min to have less of a temperature gradient.
   - Prepare 2 needles, 1 syringe and 1 filter for a syringe.
   - Go to Sharon (electron-beam physical vapor deposition machine) and prepare the machine so far, that only the sample needs to be inserted. Take the plate for the sample placement and put a sticky tape on it.
   - Use a syringe and a needle to get 1 ml of NH_4S_x. Then turn the syringe, take away the used needle, put the filter and a new needle onto the syringe and push the NH_4S_x through the filter into the 10 ml DI water which is on the hot plate at 40 °C. This cleans the NH_4S_x solution.
   - Put the sample into the NH_4S_x, DI water mixture for 150 s.
   - Then put the sample into the first 250 ml beaker, to dilute the NH_4S_x and do the same again in the second 250 ml beaker.
   - Put the sample on the sample holder for Sharon and transfer the sample as quickly as possible into the evaporation chamber of Sharon and start to pump on it.

7. Evaporation of Ti/Au

   - Evaporate 5 nm of Ti and then 55 nm of Au.

6.1.5 Lift-off

8. Metal Lift-off

   - Put the sample into ACE (50 °C) for at least two hours.

- Do turbulences with plastic pipettes to blow off the metal.
- Sonicate the sample at 20% for 30 s, check by eye if there are still regions where the metal should not be. If necessary, redo this step.
- Put the sample into IPA for 1 min.
- Blow dry sample with N_2.
- Check with the optical microscope if the lift-off worked. If not, put it back into ACE and sonicate at 20% for another 30 s, do this till the lift-off is fine.

6.1.6 Atomic Layer Deposition

9. Clean Sample
   - Clean the sample as described in Section 6.1.1.
10. Spinning Bilayer Resist
    - Spin PMMA/MMA 33% 617.08 (6'000 rpm, step size 4, 40 s).
    - Bake for 5 min at 180 °C.
    - Spin PMMA 679.03 (3'500 rpm, step size 4, 40 s).
    - Bake for 5 min at 180 °C.
    - Add 50 nm Au particles with a toothpick in each corner of the sample.
    - Check under light microscope the resist for even coating and measure the distances from the edges to the Au puddles and the tungsten alignment markers.
11. Atomic Layer Deposition (ALD)
    - Prepare a GDS file which writes a square over the NW, but not over the contact pads.
    - Put sample into SEM, set up focus, angle correction and do alignments on the tungsten markers.
    - Do EBL with 10 kV, dose 140 μC/cm^2 and aperture 120 μm for 2 mm field.
    - Do development according to point four and RIE according to point five in Section 6.1.2, respectively Section 6.1.3.
    - Preheat RIE for the desired deposition.
    - Insert sample and select the recipe for HfO_2, respectively for Al_2O_3.

– Recipe HfO_2 First Batch:

  - Set heater temperature of sample holder to 200 °C. Pulse water 0.015 s, wait 10 s, pulse TDMAH 0.2 s, wait 15 s, repeat this 250 times, resulting in a ∼30 nm thick dielectric.

– Recipe HfO_2 Second Batch:

  - Set heater temperature of sample holder to 200 °C. Pulse TDMAH 0.2 s, wait 15 s, pulse water 0.015 s, wait 10 s, repeat this 250 times, resulting in a ∼30 nm thick dielectric.

– Recipe Al_2O_3 180 °C:

  - Set heater temperature of sample holder to 180 °C. Pulse water 0.05 s, wait 12 s, pulse TMA 0.04 s, wait 10 s, repeat this 250 times, resulting in a ∼40 nm thick dielectric.

– Recipe Al_2O_3 200 °C:

  - Set heater temperature of sample holder to 200 °C. Pulse water 0.05 s, wait 12 s, pulse TMA 0.04 s, wait 10 s, repeat this 250 times, resulting in a ∼40 nm thick dielectric.

6.1.7 Lift-off ALD Window

12. ALD Lift-off

– Put sample into ACE (60 °C) for at least two hours.

– Do turbulences with plastic pipettes to blow off the resist with the oxide on top.

– Sonicate the sample at 20% for 90 s, check by eye if there are still regions where resist is, if so redo this step.

– Put sample into IPA for 1 min.

– Blow dry with N_2.

– Check with the optical microscope if the lift-off worked. If not, put it back into ACE and sonicate at 20% for another 30 s, do this till the lift-off is fine.

6.1.8 Spinning PMMA and EBL of Gate Structures

13. Spinning PMMA for Gates

– Do the same as described in step 1 and 2 in Section 6.1.1.

14. EBL for Gates

    - Prepare GDS files for writing the gates. Here, the gates are defined in the GDS with a width of 75 nm resulting in gates of 90 nm.
    - Put sample into SEM, set up focus, angle correction and do alignments on the tungsten markers.
    - Do EBL with 30 kV, dose 200 μC/cm^2 and aperture 120 μm for 2 mm field, respectively 30 kV, dose 300 μC/cm^2 and aperture 10 μm for 400 μm field.

6.1.9 Develop & RIE & Evaporation & Lift-off for Gates

15. Develop Gates

    - Do the same as described in step four Section 6.1.2.

16. RIE Gates

    - Do the same as described in step five Section 6.1.3.

17. Evaporation of Ti/Au Gates

    - Do the same as described in step seven Section 6.1.4. For the gates we do not need to get rid of the oxide and therefore we do not need the NH_4S_x-etching process.

6.1.10 Glue to Chip Carrier & Bonding

18. Cleaving Sample

    - In case that the sample is too big to fit into the chip carrier, it needs to be cleaved.
    - Do this in a hood with good ventilation and wear goggles, due to the GaAs microparticles.
    - Use a lattice scriber to make a scratch at the edge where one wants to cleave the chip.
    - Put the sample on a glass slider and position the chip so that the cleavage scratch is just no more on the glass slider. Put some force on both sides of the chip, it should cleave along the scratch.
    - Use N_2 to blow off the breaking residues.
    - Clean the chips according to Section 6.1.1.

19. Chip Carrier Cleaning

    - Put chip carrier into ACE for 5 min.
    - Sonicate the chip in ACE for 5 min at 100%.
    - Put chip carrier into IPA for 5 min.
    - Blow dry with N_2

20. Glue Sample to Chip Carrier

    - Give the Leitsilber a good shake.
    - Try to make small dots of Leitsilber glue with a toothpick on a piece of glass.
    - Check the orientation so that the flat corner of the chip holder is in the top right place.
    - Then put a small drop of glue in the middle of the chip holder and place the sample in it.
    - Use a clean toothpick and press the sample down in all corners to glue it as flat as possible to the holder.
    - Leave the glue to dry for about 2 h.

21. Bonding the Sample with Au

    - Bond the sample using an Au bonder.

6.2 Fabrication Recipe for Samples: Optimizing Conditions in Order to See Ballistic Transport

Here the fabrication recipe for the samples described in Section 3.2 is listed. We used similar recipe as for Section 3.1, respectively Section 6.1. The only things that were changed are listed below:

- GDS files for contacts was different: the contact separation were defined as 440, 340, 240 and 140 nm. This results in contact separation of 400, 300, 200, and 100 nm.
- For the ALD only HfO_2 was used. The number of layers was varied. One sample had 100 layer (∼14 nm), another 150 layer (∼21 nm) and a third 200 layer (∼28 nm) of HfO_2 deposited.
- The size of the gates was reduced to about 60 nm, by defining them 25 nm, spinning the PMMA 4.5% by 5'000 rpm for 40 s and increasing the dose to dose 400 $\mu C/cm^2$, 30 kV, and aperture 10 μm for 400 μm field.

6.3 Fabrication Five Gate Structures

The recipe for the fabrication of the five gate structures seen in Figure 20a is described.

6.3.1 Prepare Resist

1. Cleaning
   - 5 min in acetone (ACE).
   - 5 min in isopropanol (IPA).
   - Blow dry with N_2.
   - Put on hot plate 2 min at 120 °C.
2. Spinning PMMA
   - Spin 1.8% PMMA (6'000 rpm, step size 4, 45 s).
   - Bake for 5 min at 180 °C.
   - Second time, spin 1.8% PMMA (6'000 rpm, step size 4, 45 s).
   - Bake for 5 min at 180 °C.
   - Add 50 nm Au particles with a toothpick in each corner of the sample.
   - Check under light microscope the resist for even coating and measure the distances from the edges to the Au puddles and the tungsten alignment markers.

6.3.2 Electron Beam Lithography of five Gates & Development

3. EBL
   - Prepare GDS files for writing the single pixel lines for the gate, the gates are defined to be separated by 75 nm which results in a separation of 40 nm.
   - Put sample into SEM, set up focus, angle correction and do alignments on markers.
   - Do EBL with 30 kV, dose 4750 pC/cm^2 and aperture 7.5 μm for a 50 μm write field.
4. Development
   - Use dried ice to cool down the developer ((MIBK + IPA) : MEK, ration 100:1.3) to $-18.5\,^{\circ}$C.
   - Put sample into developer ((MIBK + IPA) : MEK, ration 100:1.3) for 30 s.
   - Blow dry with N_2 for at least 1 min.

6.3.3 Evaporation & Lift-off of Gates

5. Evaporation of Ti/Pd Gates
   - Evaporation of 1 nm Ti as a sticking layer, followed by 9 nm of Pd.
6. Lift-off
   - Do the same as described in Section 6.1.5

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